

REMARKS

Claims 1-6 and 8-17 are pending in the application. In the Final Office Action of February 14, 2003, the Examiner made the following disposition:

- A.) Required corrected Figure 1.
- B.) Objected to claim 8.
- C.) Rejected claims 1, 3-6, 8 and 11-17 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Koch*.
- D.) Rejected claim 2 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Koch* and further in view of *Gowda*.
- E.) Rejected claims 9 and 10 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Koch* and further in view of *Munier*.

Applicants respectfully traverse the rejections and address the Examiner's disposition as follows:

A.) Requirement for corrected Figure 1:

As per the Examiner's request, Applicants here with submit a corrected Figure 1.

Applicants respectfully submit the requirement has been fulfilled and request that it be withdrawn.

B.) Objection to claim 8:

Claim 8 has been cancelled.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

C.) Rejection of claims 1, 3-6, 8 and 11-17 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Koch*:

Applicants respectfully disagree with the rejection.

Claims 1, 14 and 16 have each been amended to include the subject matter of claim 8. Claim 8 has accordingly been cancelled.

Applicants' independent claims 1, 14 and 16, each as amended, each claim a selection switch and a read-out switch that each comprises a MOS transistor having a double gate structure, wherein each gate electrode of the selection switch and the read-out switch comprises a two-layer gate electrode, and neighboring portions that are overlapped with each other.

Referring to Applicants' Figure 4 for illustrative purposes, as claimed, neighboring portions of the gate electrodes 13a, 14a of the selection MOS transistor 13 and the read-out MOS transistor 14 are overlapped with each other, whereby the n+ diffusion region does not occur between the gate electrodes 13a, 14a. Accordingly, a noise component due to the dispersion of the field occurring in the gate electrode 14a of the read-out MOS transistor 14 at the shift timing from the period d to the period e is completely transferred. Therefore, any noise due to the gate electrode 14a of the read-out MOS transistor 14 does not occur.

Further, the overflow charge from the photodiode 12 is directly supplied to the n+ diffusion region connected to the vertical signal line 15, so that smear can be suppressed to only the charges occurring within the one pixel read-out time by resetting the vertical signal line 15 just before the signal charge (pixel signal) is read out. (See page 12, paragraph 3 - page 14, paragraph 1).

This is clearly unlike *Sauer* in view of *Koch*, which fails to disclose or suggest each gate electrode of a selection switch and a read-out switch that comprises a two-layer gate electrode and neighboring portions that are overlapped with each other. As stated by the Examiner, *Sauer* fails to disclose a double-gated transistor. Therefore, the Examiner combines *Sauer* with *Koch* in an attempt to disclose or suggest claims 1, 14 and 16, however, Applicants respectfully submit that *Sauer* in view of *Koch* still fails to disclose or suggest claims 1, 14 and 16, as amended.

Although *Koch* discloses a double-gated transistor, *Koch* still fails to disclose or suggest each gate electrode of a selection switch and a read-out switch that comprises a two-layer gate electrode and neighboring portions that are overlapped with each other. Accordingly, *Sauer* in view of *Koch* still fails to disclose or suggest claims 1, 14 and 16.

Claims 3-6, 11-13, 15 and 17 depend directly or indirectly from claims 1, 14 or 16 and are therefore allowable for at least the same reasons that claims 1, 14 and 16 are allowable. Claim 8 has been cancelled.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

D.) Rejection of claim 2 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Koch* and further in view of *Gowda*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 is allowable over *Sauer* in view of *Koch* as described above. *Gowda* still fails to disclose or suggest each gate electrode of a selection switch and a read-out switch that comprises a two-layer gate electrode and neighboring portions that are overlapped with each other. Therefore, *Sauer* in view of *Koch* and further in view of *Gowda* still fails to disclose or suggest claim 1.

Claim 2 depends directly or indirectly from claim 1 and is therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

E.) Rejection of claims 9 and 10 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Koch* and further in view of *Munier*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 is allowable over *Sauer* in view of *Koch* as described above. *Munier* still fails to disclose or suggest each gate electrode of a selection switch and a read-out switch that comprises a two-layer gate electrode and neighboring portions that are overlapped with each other. Therefore, *Sauer* in view of *Koch* and further in view of *Munier* still fails to disclose or suggest claim 1.


Claims 9 and 10 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-6 and 9-17 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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In the Claims:

Please amend claims 1, 14 and 16 as follows:

1. (Twice Amended) A solid-state image pickup device, comprising:

a pixel portion having unit pixels arranged two-dimensionally in a matrix form, each of said unit pixels including a photoelectrically transducing element for photoelectrically transducing incident light to obtain a signal charge, and stocking the signal charge thus obtained, a selection switch for selecting one of the pixels, and a read-out switch for reading out the signal charge from said photoelectrically transducing element to one of a plurality of vertical signal lines;

a plurality of amplifying means, at least one of the amplifying means being connected to each of said respective vertical signal lines and for converting the signal charge read out to the vertical signal lines to an electrical signal; and

a plurality of reset means for resetting each of said vertical signal lines;

wherein each of said selection switch and said read-out switch comprises a MOS transistor having a double gate structure, and

wherein each gate electrode of said selection switch and said read-out switch comprises a two-layer gate electrode, and neighboring portions are overlapped with each other.

14. (Twice Amended) A method of driving a solid-state image pickup device comprising a pixel portion having unit pixels arranged two-dimensionally in a matrix form, each of said unit pixels including a photoelectrically transducing element for photoelectrically transducing incident light to obtain a signal charge and stocking the signal charge thus obtained, a selection switch for selecting one of the pixels, and a read-out switch for reading out the signal charge from said photoelectrically transducing element to one of a plurality of vertical signal lines; a plurality of amplifying means at least one of which are connected to each of said respective vertical signal lines and for converting the signal charge read out to the vertical signal lines to an electrical signal, and a plurality of reset means for resetting each of said vertical signal lines, the method comprising the steps of:

resetting the vertical signal line;

after resetting the vertical signal line, reading out a pixel signal from said photoelectrically transducing element to the vertical signal line to successively output a reset level and a signal level in this order through the same route; and

after reading out the pixel signal, calculating a difference between the reset level and the signal level, wherein each of said selection switch and said read-out switch comprises a MOS transistor having a double gate structure,

wherein each gate electrode of said selection switch and said read-out switch comprises a two-layer gate electrode, and neighboring portions are overlapped with each other.

16. (Twice Amended) A camera comprising:

an optical system for focusing incident light from a subject onto a solid-state image pickup device;

a driving system for driving said solid-state image pickup device; and

a signal processing system for processing an output signal of said solid-state image pickup device, wherein said solid-state image pickup device comprises a pixel portion having unit pixels arranged two-dimensionally in a matrix form, each of said unit pixels including a photoelectrically transducing element for photoelectrically transducing incident light to obtain signal charge, and stocking the signal charge thus obtained, a selection switch for selecting one of the pixels, and a read-out switch for reading out the signal charge from said photoelectrically transducing element to one of a plurality of vertical signal lines, a plurality of means, at least one of which are connected to each of said respective vertical signal lines and for converting the signal charge read out to the vertical signal lines to an electrical signal, and a plurality of reset means for resetting each of said vertical signal lines, and wherein said driving system drives said solid-state image pickup device so that one of the vertical signal lines is first reset and then a pixel signal is read out from said photoelectrically transducing element to the vertical signal line to successively output a reset level and a signal level in this order through the same route, and thereafter calculates a difference between the reset level and the signal level, and wherein each of said selection switch and said read-out switch comprises a MOS transistor having a double gate structure, and

wherein each gate electrode of said selection switch and said read-out switch comprises a two-layer gate electrode, and neighboring portions are overlapped with each other.

Please cancel claim 8.